APPENDIX K

A fixed logic zero signal is coupled at node 852 to an input of a shift register comprising flip-flops 866, 868, 870, and 872. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 854. A transmit clock signal is provided to a clock input of the shift register at node 856. Nodes 858, 860, 862, and 864 are coupled to parallel load data inputs of flip-flops 866, 868, 870, and 872, respectively. A serial data output of the shift register at the output of flip-flop 872 is coupled to an input of multiplexer 876 at node 874.

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